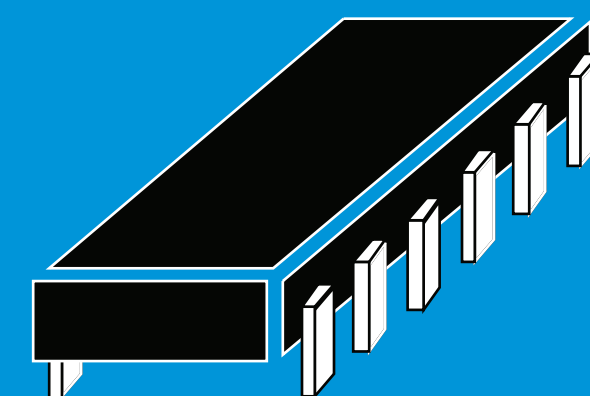




Low power & High performance

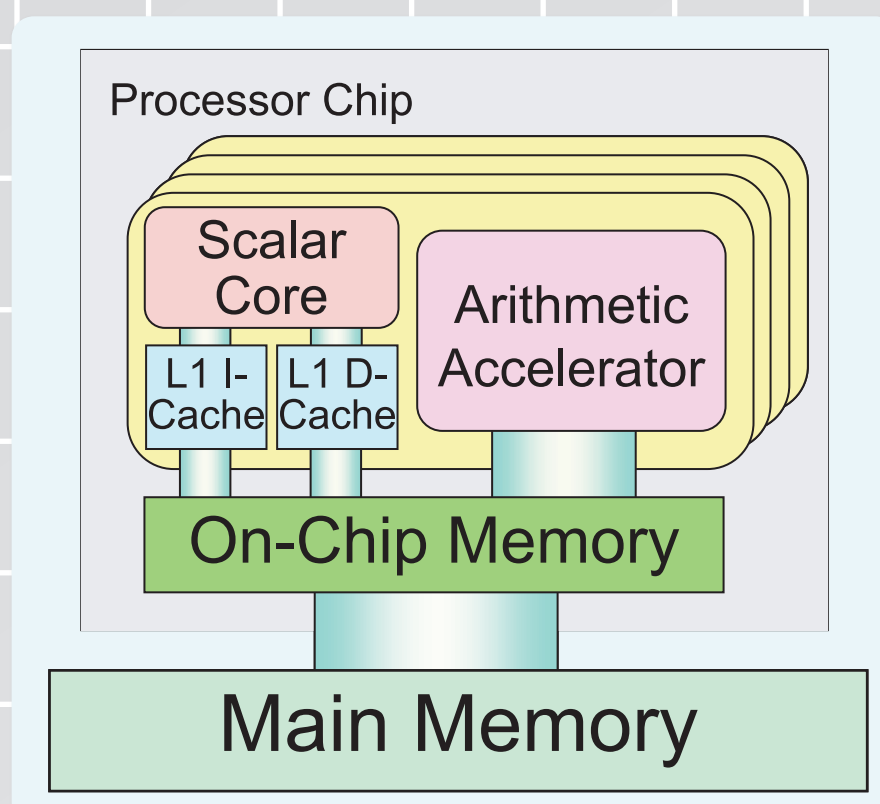
On-Chip Memory Processor with Arithmetic Accelerators

Processor Design

Overview

We adapt arithmetic accelerators to on-chip memory processor, which is expected to improve power performance.

- On-chip memory
 - It assumes **SCIMA** processor
 - It is shared with processor cores
- Arithmetic accelerator
 - Higher performance/energy
 - SIMD-type or Vector-Type
- Multi-core processor
 - A core includes an arithmetic accelerator, a scalar core and L1-I&D caches



SCIMA: Our On-Chip Memory Architecture

Advantage of SCIMA:

Software Controlled Integrated Memory Architecture Performance Improvement

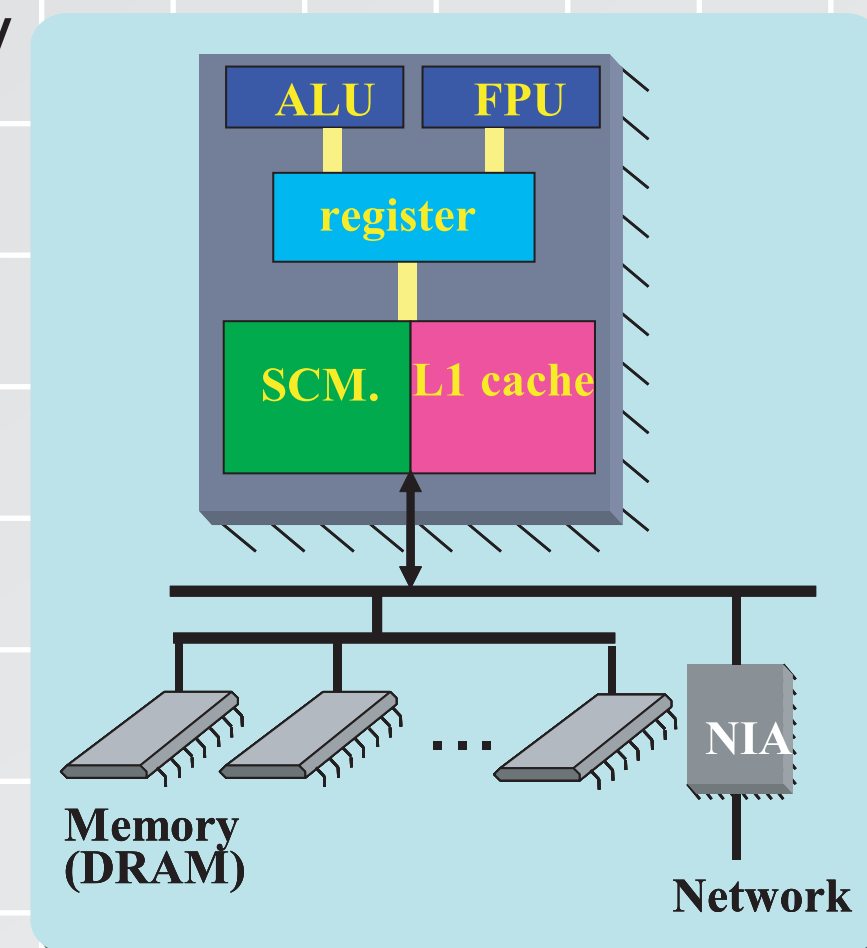
- full exploitation of data locality without cache pollution
- flexible granularity of data transfers from/to off-chip memory

Dynamic Power Reduction

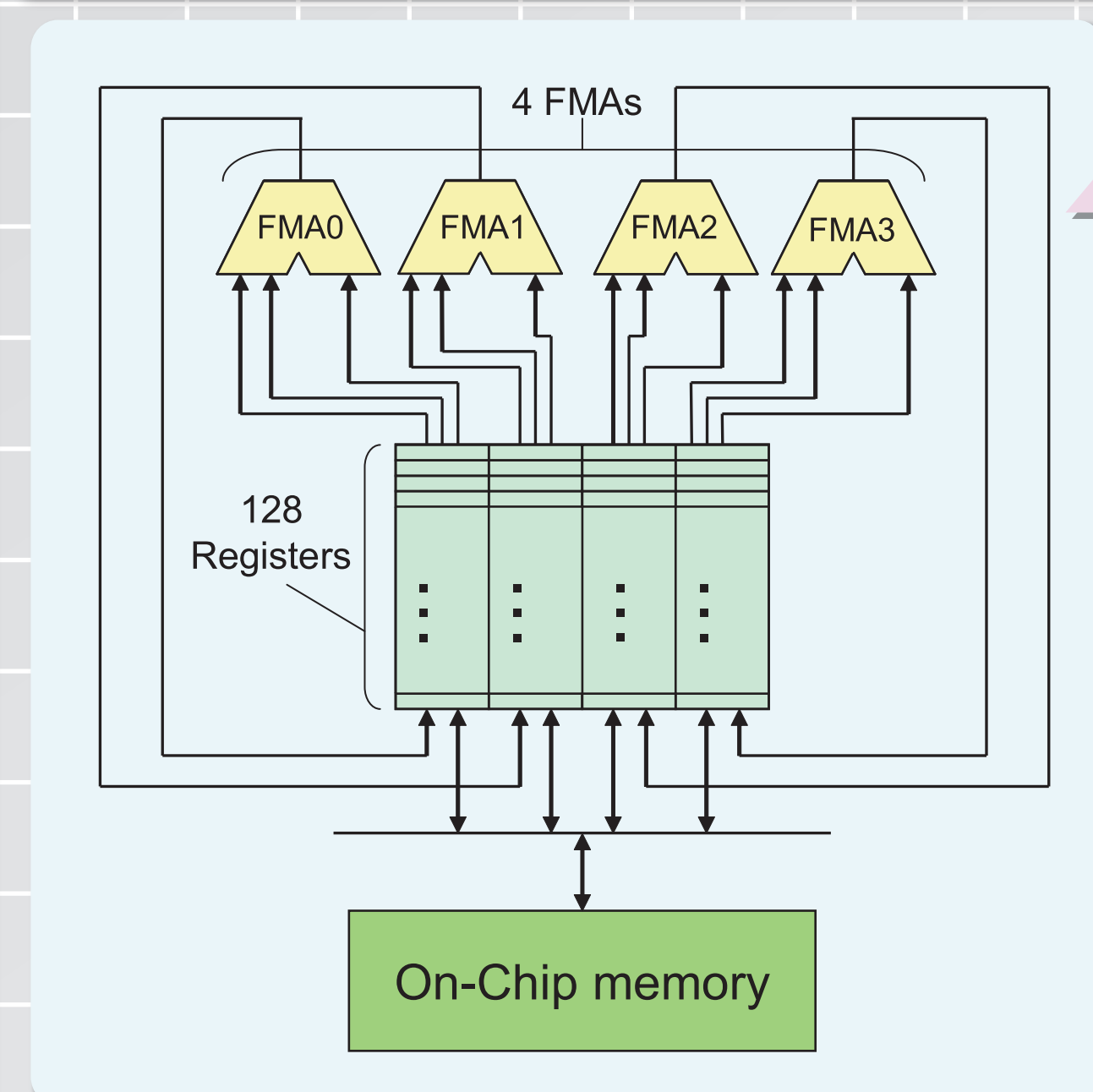
- by reduced off-chip access

Static Power Reduction

- identification and Vdd gating of unnecessary on-chip memory area



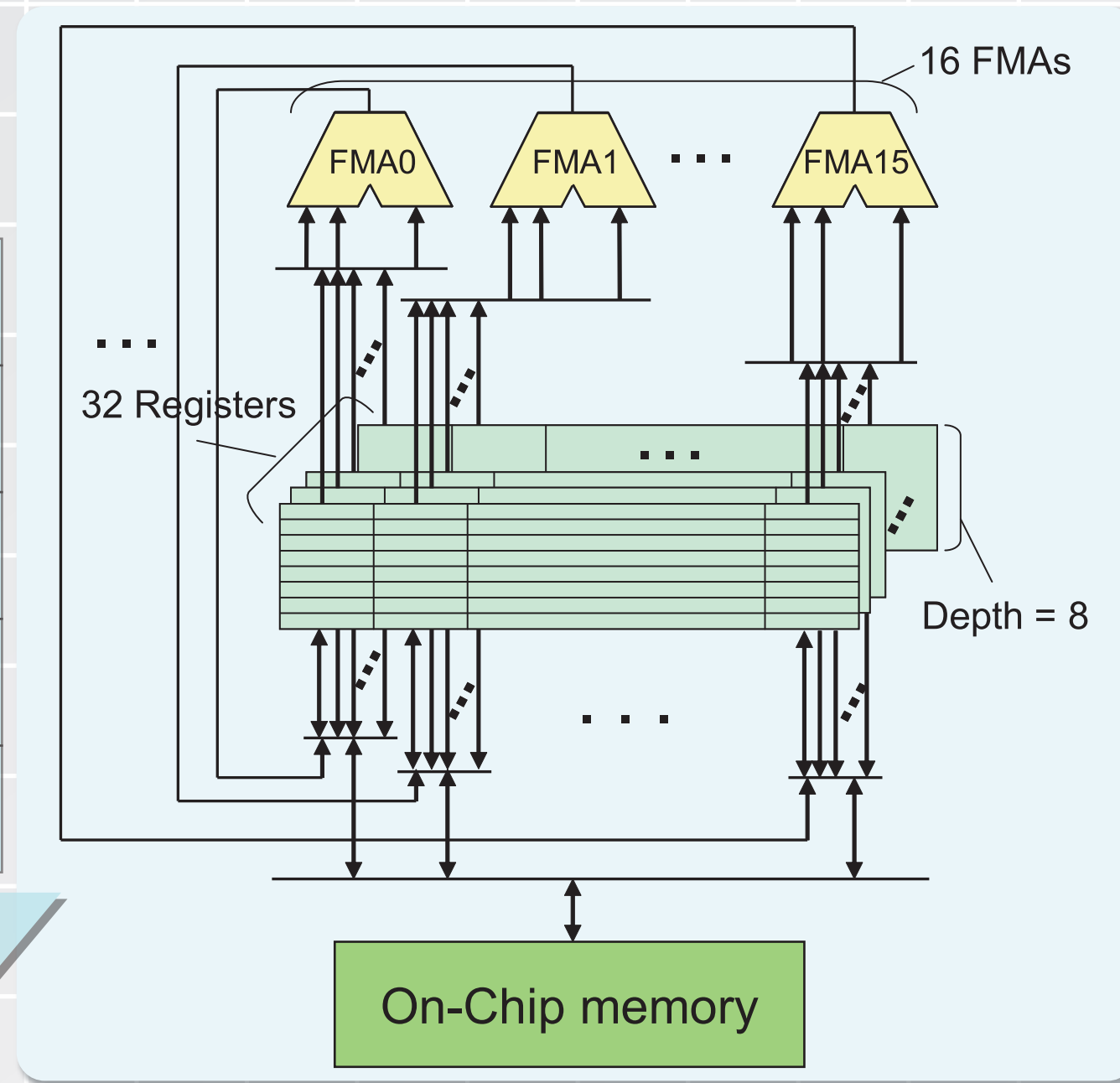
Arithmetic Accelerators



SIMD-type accelerator

4	Fused Multiply-Adder	16
128 registers * (4elem. * 64bit)	Registers	32 registers * (128elem. * 64bit)
Yes	Inter-elements Calculation	No
8 MB	On-Chip Memory	8 MB
2.0 GHz	Core clock	2.0 GHz

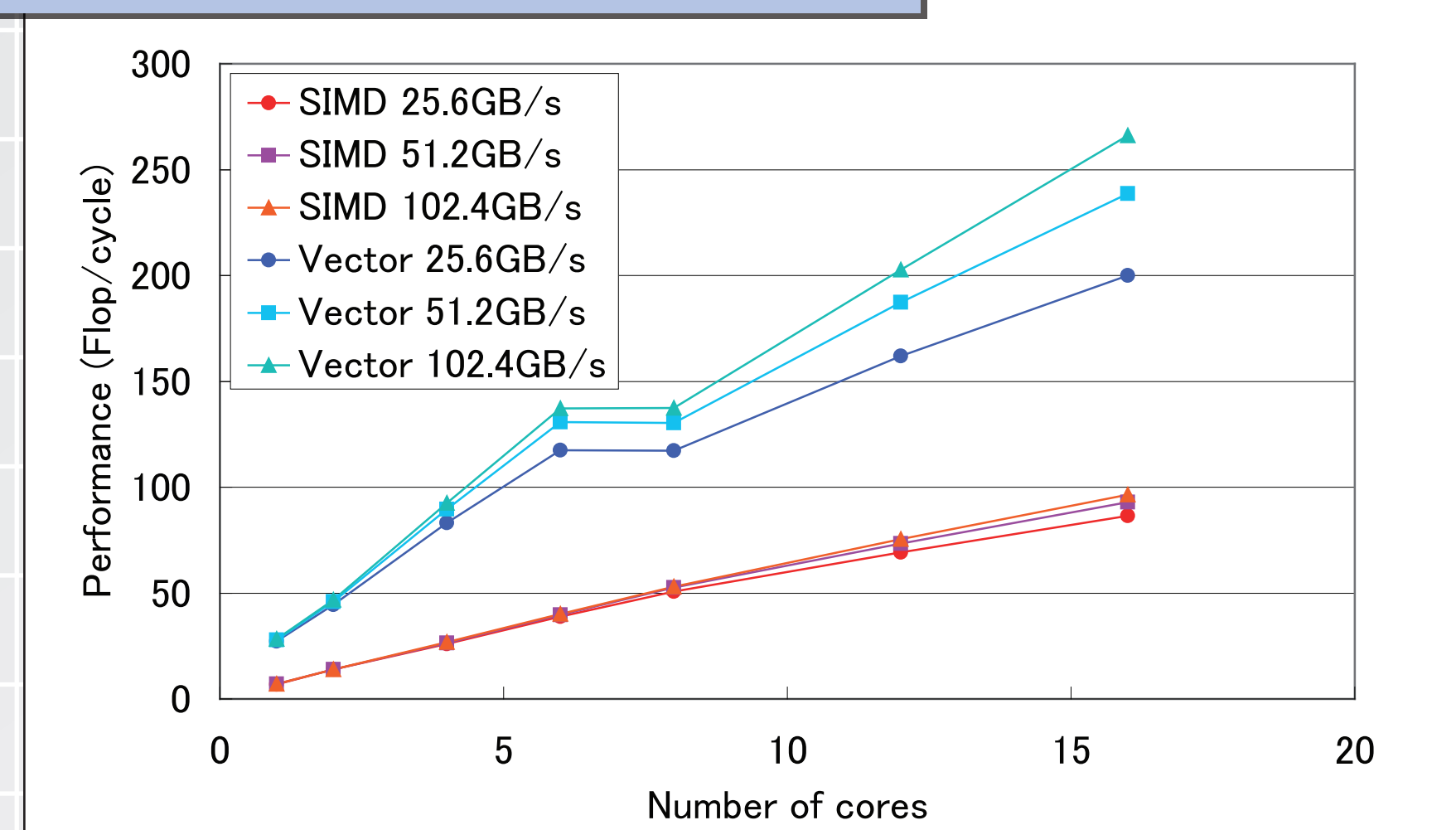
Vector-type accelerator



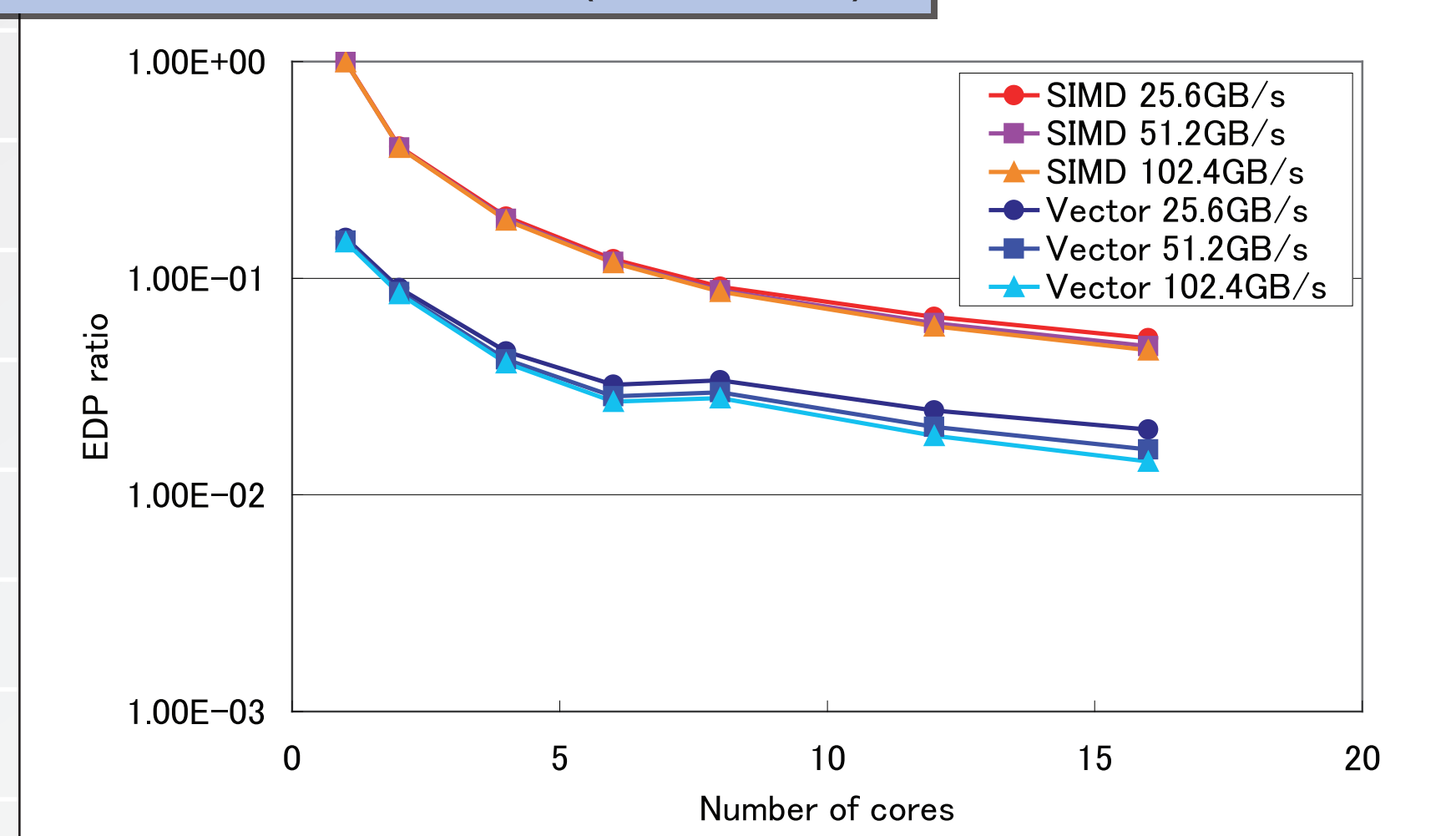
Performance Simulation Results

Matrix multiplication ($N=1728^2$)

Practical Performance (Flop/cycle)



Power Performance (EDP ratio)



Each type of the On-Chip Memory Processor with Arithmetic Accelerators achieves good performance and scalability. However, the vector-type has advantage on EDP per FMA. We need further simulations of various applications, some of which take advantages of SIMD-type's feature.

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