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High-Performance & Low-Power Parallel Platform for Dependable Embedded Systems

Overview

We propose a low-power and high-performance parallel platform for dependable embedded systems using multi-core processor and multi-processor.

- Multi-processor Platform
  - SiP (System In Package) Module
    - CPU: Renesas SH-4A
  - Low-power & high-speed communication link
  - Cooperative development with Renesas Tech.
- OpenMP Programming Environment
  - Reliable Software-DSM
  - Remote Checkpoint/Restart Scheme
- Runtime system for power management
  - Low-power under real-time constraint

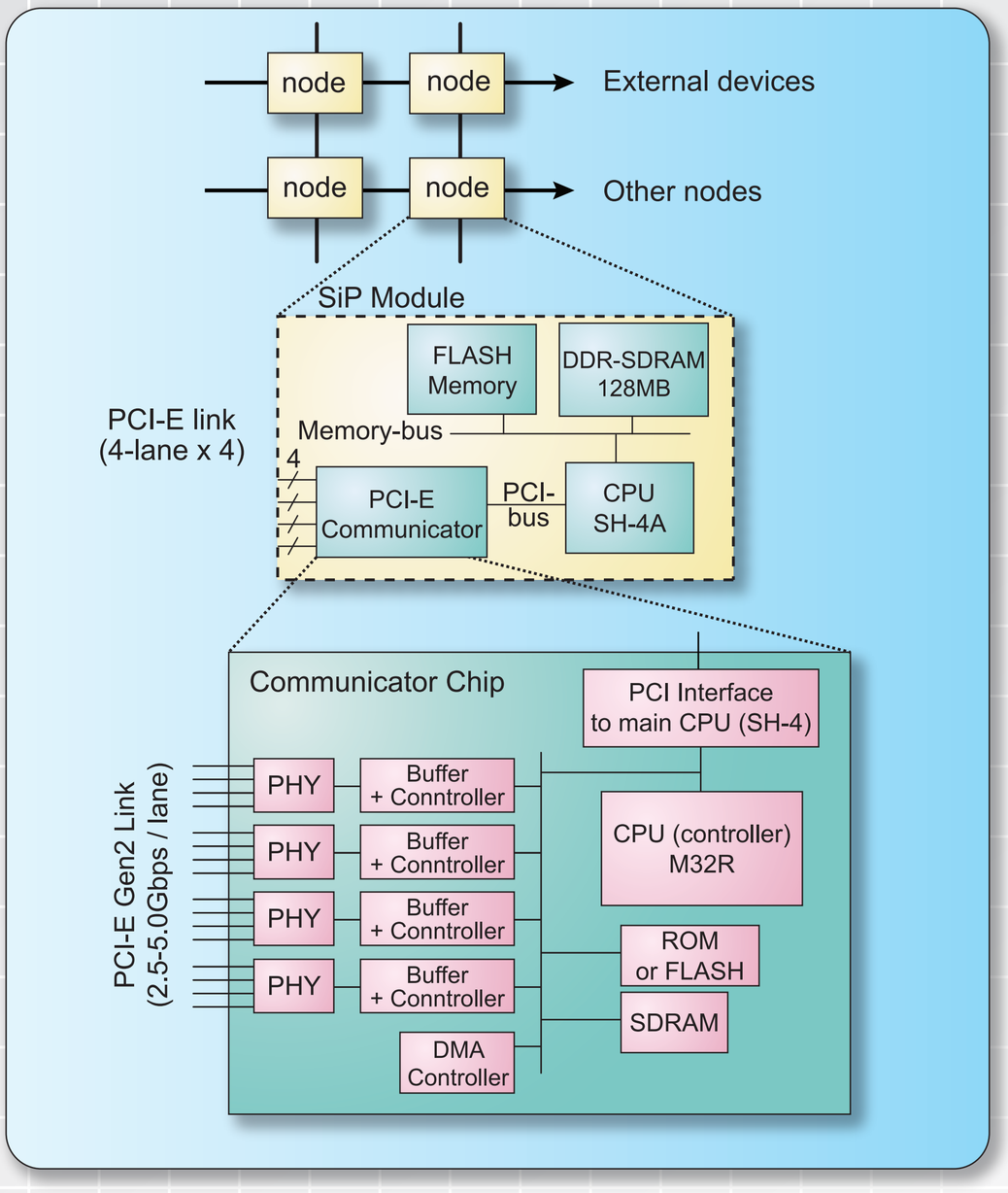
Low-power & High-speed Communicator Chip

Link: [PCI Express Gen2 x4 lane] x 4 direction

- Available # of lanes is selectable (x1,x2,x4) for performance/power balance
- Gen2 (5Gbps/lane) <-> Gen1 (2.5Gbps/lane)
  - Maximum bandwidth:
    - 20Gbps/dir. -> 2GB/s (8B10B enc.)

CPU(Controller): Renesas M32R

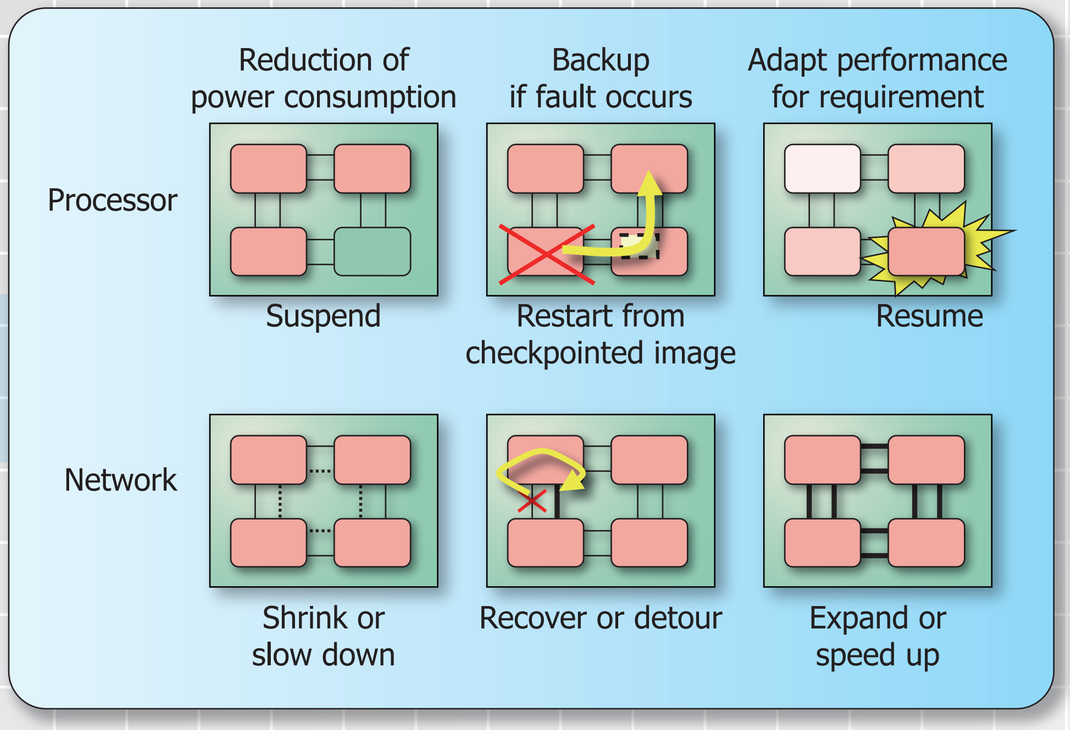
- Handling in-coming packet header, and forwards to destination (routing function)
- PCI Express Gen2 compatible header creation
- Fast switching with DMA for payload



Concept of Management for Dependability and Performance / Power

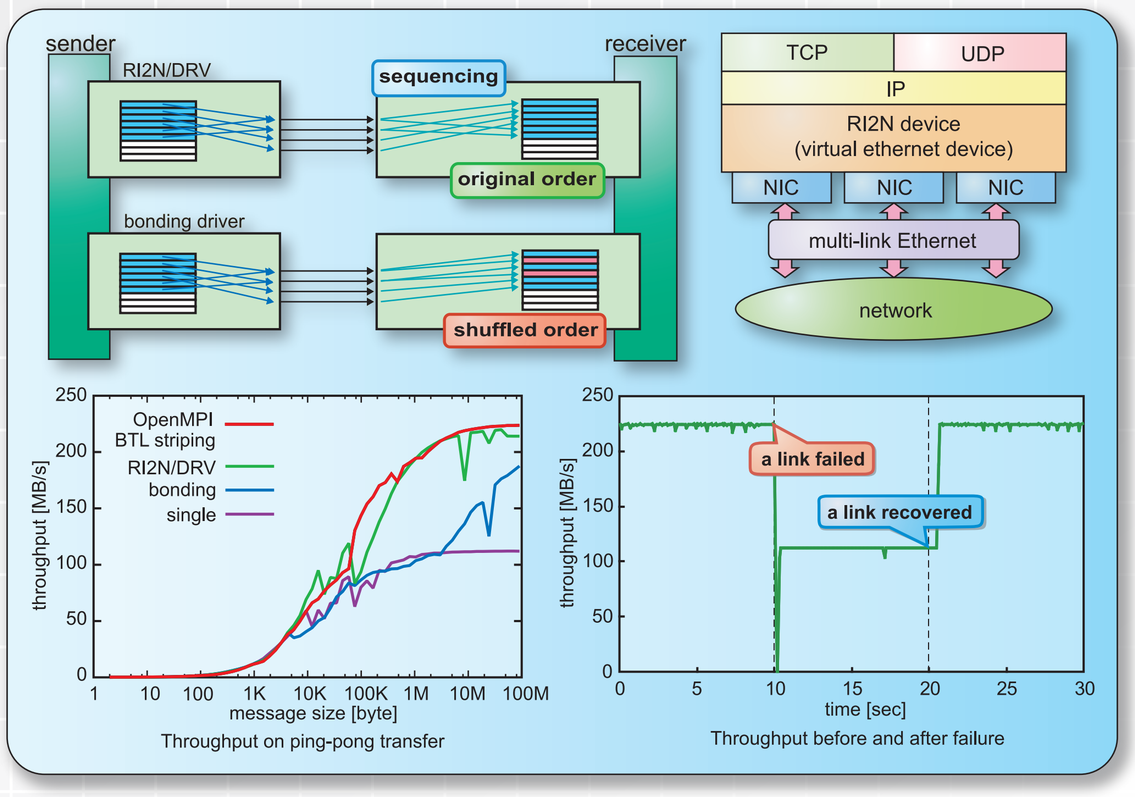
For the both of processors and interconnection network, our system provides:

- High Quality
  - High-performance, Real-time, Low-power
- High Dependability
  - Reliability, Availability, Fault-tolerance



RI2N
(Redundant Interconnection with Inexpensive Network)

- Utilizes multiple links of commodity networks to achieve both high-bandwidth and high-dependability
- Trunking multiple links to improve the bandwidth and enhances the link failure detection
- RI2N/DRV is a user-transparent implementation of RI2N on virtual Ethernet device driver, similar to Channel Bonding Driver
- RI2N/DRV provides a packet sequencing function to avoid the misinterpretation on TCP/IP layer for non-consequent packets on single channel



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